Dear Customer,

Following the continuous improvement of our service and in order to increase the productivity, this document is announcing that PowerFLAT™ 5x6 products, listed in this PCN, will be also produced in our Subcontractor Tongfu Microelectronics (China) (Ex Nantong Fujitsu Microelectronics).
Tongfu Microelectronics subcontractor is our preferred partner for power packages since long time. Devices used for qualification are available as samples.

PowerFLAT™ 5x6 package produced in Tongfu Microelectronics FAB, guarantees the same quality and electrical characteristics as per current production.

The involved product series and affected packages are listed in the table below:

Product Family	Package	Commercial Product / Series
Power MOSFET Transistors	PowerFLAT™ 5x6	STLxxx

Any other Product related to the above series, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 21-2017.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power MOSFET Transistors	PowerFLAT™ 5x6	STL220N3LLH7 STL150N3LLH6 STL150N3LLH5

Change implementation schedule:

The production start and first shipments will be implemented after week 34 of 2017.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of PowerFLAT™ 5x6 products, manufactured in Tongfu Microelectronics subcontractor (China), will be ensured by "GF" as first digits of the trace code, internal code (Finished Good) and Q.A. number.

Yours faithfully.

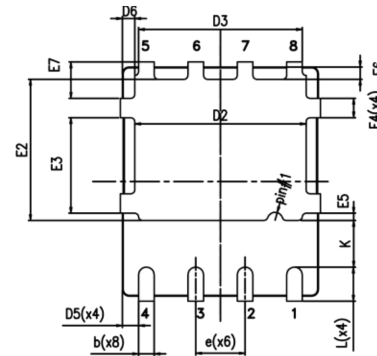
PowerFLAT™ 5x6 Clip Bonding (type C)

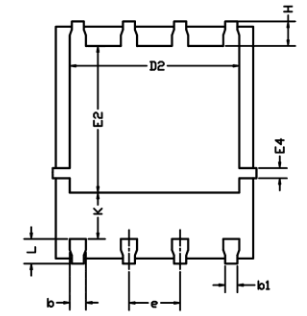
STMicroelectronics Vs Tongfu Microelectronics

DIMENSIONS (mm)							
ST				TFME			
REF. DIM	NOM	MIN	MAX	NOM	MIN	MAX	REF. DIM
A		0.80	1.00	0.95	0.90	1.00	A
A1		0.02	0.05	0.02			A1
A2	0.25			0.25	0.21	0.34	c
b		0.30	0.50	0.40	0.35	0.45	b
b1				0.30			b1
C	6.00	5.80	6.20	5.75	5.70	5.80	E1
D	5.20	5.00	5.40			5.10	D
D2		4.15	4.45	4.21	4.01	4.31	D2
D3	4.20	4.05	4.35				
D4	5.00	4.80	5.20	4.90	4.80	5.00	D1
D5	0.40	0.25	0.55				
D6	0.30	0.15	0.45				
e	1.27			1.27	1.17	1.37	e
E	6.15	5.95	6.35	6.00	5.90	6.10	E
E2		3.50	3.70	3.64	3.54	3.74	E2
E3		2.35	2.55				
E4		0.40	0.60	0.25			E4
E5		0.08	0.28				
E6	0.33	0.20	0.45				
E7	0.90	0.75	1.05				
				0.61	0.51	0.71	H
K		1.05	1.35		0.95		K
L		0.73	1.03	0.61	0.51	0.71	L
L1	0.15	0.05	0.25	0.13	0.06	0.20	L1
						0.10	L2
				1.10	1.00	1.20	P
θ		0°	12°	10°	8°	12°	θ

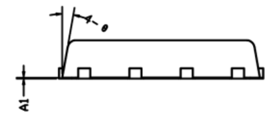
TFME

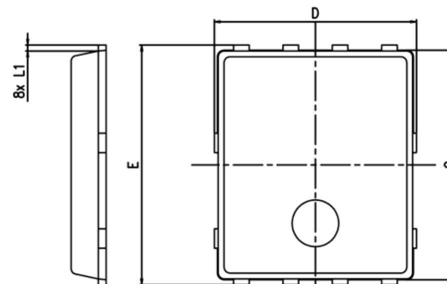
BOTTOM VIEW

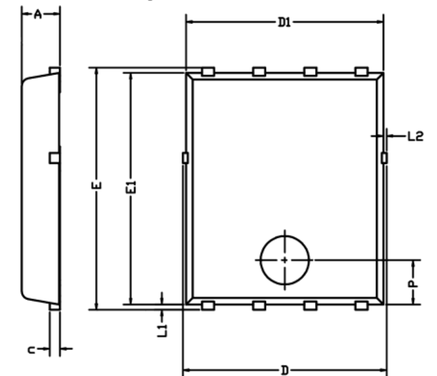




SIDE VIEW



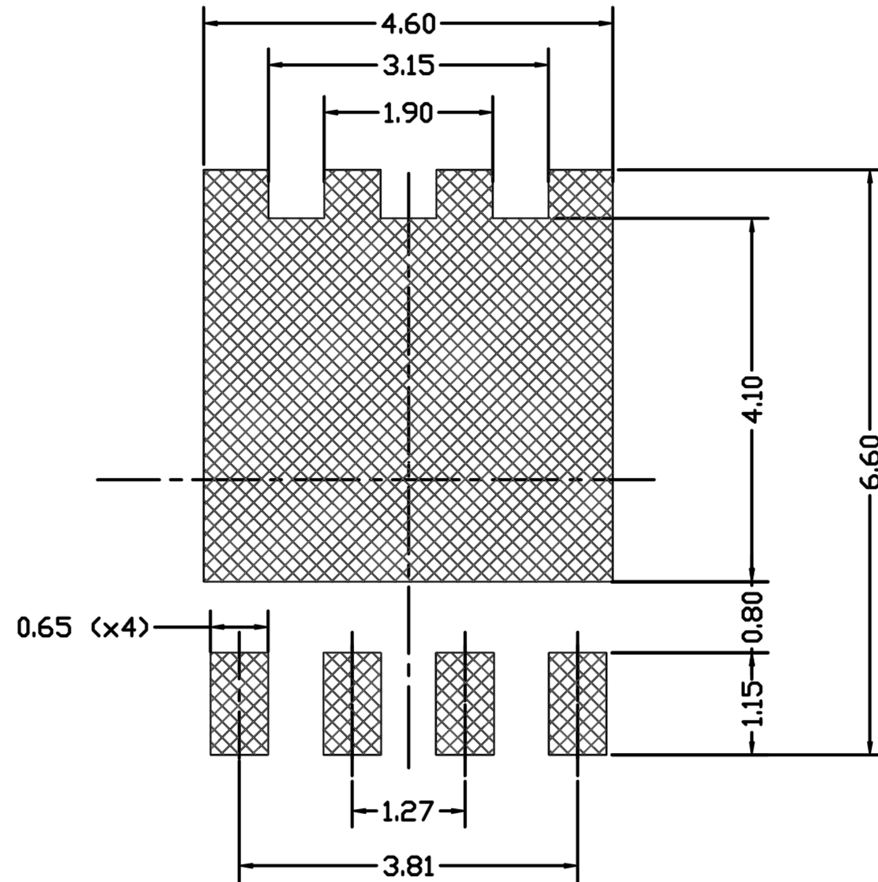




TOP VIEW

life.augmented

RECOMMENDED FOOTPRINT



Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : PowerFLAT™ 5x6 Clip Capacity Extension - Tongfu Microelectronics (China)
PCN Reference : ADG/17/10319

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STL140N6F7	STL130N6F7	STL90N6F7
STL110NS3LLH7	STL160NS3LLH7	STL150N3LLH6
STL120N8F7	STL150N3LLH5	STL160N3LLH6
STL220N3LLH7	STL100N8F7	STL90N3LLH6
STL110N10F7	STL140N4LLF5	STL260N3LLH6
STL75N8LF6		

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FINAL Reliability Report

Qualification for capacity expansion of
PowerFLAT™ 5x6 package with clip manufactured in
Tongfu Microelectronics (China)

General Information	
Product Lines:	NN3T01- 6L3F01 – 5L3T01
P/N:	STL220N3LLH7 (NN3T01) STL150N3LLH6 (6L3F01) STL150N3LLH5 (5L3T01)
Product Group:	ADG
Product division:	Power Transistor Division
Package:	PowerFLAT™ 5x6
Silicon Process techn.:	Power MOSFET

Locations	
Wafer Fab and EWS Plant:	*Wafer foundry - SCIS SEREMBAN DIFF (NN3T01)* *Catania CT8" (6L3F01 – 5L3T01)*
Assembly and testing plant:	*Tongfu Microelectronics (China)*
Reliability Lab:	*ADG - Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	June 2017	7	A. Settinieri	C. Cappello	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
This report does not imply for STMicroelectronics expressly or implicitly any contractual obligations other than as set forth in STMicroelectronics general terms and conditions of Sale. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification for capacity expansion of PowerFLAT^{TM} 5x6 package with clip and wafer thickness 100 / 200 µm manufactured in Tongfu Microelectronics (China).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. Reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

Power MOSFET

4.2 Construction note

D.U.T.: STL220N3LLH7 **PACKAGE: PowerFLAT™ 5x6**

Wafer/Die Information	
Technology	Power MOSFET STripFET™ H7
Wafer Fab	*Wafer foundry - SCIS SEREMBAN DIFF*
Wafer thickness	100 µm
Die finishing back side	Ti-Ni-Ag
Die size	3683 x 3124 μm^2
Metal	AlCu
Passivation type	None

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	PowerFLAT™ 5x6
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Pb-Sn-Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Au Source: Clip
Lead finishing/bump solder material	Pure Tin

D.U.T.: STL150N3LLH6 **PACKAGE: PowerFLAT™ 5x6**

Wafer/Die Information	
Technology	Power MOSFET STripFET™ H6
Wafer Fab	*CT8” (Italy)*
Wafer thickness	200 µm
Die finishing back side	Ti-NiV-Ag
Die size	3860 x 2640 μm^2
Metal	AlCu
Passivation type	USG/TEOS

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	PowerFLAT™ 5x6
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Pb-Sn-Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Au Source: Clip
Lead finishing/bump solder material	Pure Tin

D.U.T.: STL150N3LLH5 PACKAGE: PowerFLAT™ 5x6

Wafer/Die Information	
Technology	Power MOSFET STripFET™ H5
Wafer Fab	CT8” (Italy)
Wafer thickness	200 µm
Die finishing back side	Ti-NiV-Ag
Die size	3740 x 4070 $µm^2$
Metal	AlCu
Passivation type	USG/TEOS

Assembly/Testing information	
Assembly site	Tongfu Microelectronics (China)
Package description	PowerFLAT™ 5x6
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach material	Pb-Sn-Ag
Wire bonding process	Ultra Thermosonic
Wires bonding materials	Gate: Au Source: Clip
Lead finishing/bump solder material	Pure Tin

5 TESTS RESULTS SUMMARY

5.1 Test vehicles

Lot	Part Number	Product Lines	Wafer Fab	Assy Plant	Comments
1	STL220N3LLH7	NN3T01	*SCIS SEREMBAN DIFF*	Tongfu Microelectronics (China)	
2	STL150N3LLH6	6L3F01	*CT8" (Italy)*		
3	STL150N3LLH5	5L3T01			

5.2 Reliability test plan summary

#	Stress (Abrv)	PC	Std ref.	Conditions	Sample Size (S.S.)	Steps	Failure/SS		
							Lot 1	Lot 2	Lot 3
1	**TEST**		User specification	All qualification parts tested per the requirements of the appropriate device specification.			0/462	0/462	0/462
2	**External visual**		JESD22 B-101	All devices submitted for testing			0/462	0/462	0/462
3	**Pre-conditioning**		JESD22 A-113	Dryng 24H @ 125°C Store 168H @ TA=85°C,RH=85% IR Reflow @ 260°C 3 times		All devices to be subjected to H3TRB, TC, AC, IOL	0/308	0/308	0/308
4	**HTRB**	N	JESD22 A-108	Tj = 150°C ; BIAS = 24V	135	1000h	0/45	0/45	0/45
5	**HTGB**	N	JESD22 A-108	TA=150°C ; BIAS= 20V	90	1000H	0/45	0/45	
				TA=150°C ; BIAS= 22V	45				0/45
6	**TC**	Y	JESD22 A-104	TA=-65°C TO 150°C 1 HOURS / CYCLE	75	500cy	0/25	0/25	0/25
7	**AC**	Y	JESD22 A-102	TA=121°C ; PA=2ATM	75	96H	0/25	0/25	0/25
8	**H3TRB**	Y	JESD22 A-101	TA=85°C ; RH=85% BIAS=24V	75	1000H	0/25	0/25	0/25
9	**IOL**	Y	MIL-STD-750 Method 1037	ΔTj ≥100°C	75	15Kcy	0/25	0/25	0/25
10	**ESD**		AEC Q101-001,002 and 005	CDM / HBM	9		0/3	0/3	0/3

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
HTRB High Temperature Reverse Bias **HTGB / HTFB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
IOL / TF Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB/THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.